

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

QING MA
QUAN TRAN
STEVE TOWLE
EBRAHIM ANDIDEH

Serial No.: 10/038,343

Filed: January 2, 2002

For: A SEMICONDUCTOR DEVICE HAVING
A LOW-K DIELECTRIC LAYER

) Examiner: D. Le

) Art Unit: 2818

) Attorney Docket: 042390.P8125D

Which is a Divisional of Application:)

Serial No.: 09/524,766

Filed: March 14, 2000

) Examiner: D. Le

) Art Unit: 2818

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF MARK V. SEELEY
UNDER 37 C.F.R. § 1.131

Dear Sir:

I, Mark V. Seeley, declare that:

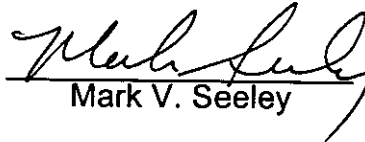
1. I am a patent attorney with Intel Corporation, the assignee of the captioned non-provisional patent application.
2. I understand that the Intel legal department received – no later than November 15, 1999 – an invention disclosure, dated October 4, 1999, that described a multilayer laminate for use in a semiconductor device. The invention disclosure illustrated a two layer laminate that included a carbon doped oxide layer and a tougher film that was under compressive stress such as silicon dioxide or silicon nitride, and illustrated a four layer laminate that included a first carbon doped oxide layer, a first thin coating of the tougher film, a second carbon doped oxide layer, and a second thin

coating of the tougher film. Attached as Exhibit A is a true and correct copy of that invention disclosure.

3. The invention disclosure was assigned to an Intel invention review committee for evaluation. After meeting to review that invention disclosure, along with many others, the committee authorized the filing of a patent application for the invention.
4. The application was subsequently assigned to me for drafting. Soon after receiving the file, I began drafting a patent application for the invention described in the invention disclosure. After the inventors concluded that a draft accurately and completely described their invention, they signed Declaration and Power of Attorney forms for the application, and assignments for it, and returned those documents to me. Attached as Exhibits B, C, D, and E are true and correct copies of those documents.
5. After receiving the Declaration and Power of Attorney forms and the assignments, I had the parent application for the pending patent application filed on March 14, 2000.
6. I drafted the patent application that issued as United States Patent No. 6,383,917. That patent application and the pending patent application were, at the time the invention claimed in the pending patent application was made, subject to an obligation of assignment to the same entity – namely Intel Corporation.
7. This declaration is being submitted to support a response to an Office Action mailed on October 21, 2004 for U.S. Patent Application Serial Number 10/038,343 entitled "A Semiconductor Device Having a Low-K Dielectric Layer."

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the captioned application or any patent issued thereon.

Date: December 9, 2004


Mark V. Seeley

TMG INVENTION DISCLOSURE, Rev 1, 2/98

Located at: <http://legal.intel.com>LEGAL ID# 13080 (legal dept. use only)

DATE:

NOV 10 1999

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval. If you have any questions regarding this form or to whom it should be forwarded, please call 503-264-0444.

Fill out the below and follow the instructions:

1. Field of the Invention:
- ☒ Semiconductor Process: device and integration
 - ☐ Semiconductor Process + Equipment: thin films
 - ☐ Semiconductor Process + Equipment: etch/litho
 - ☐ Circuit Design
 - ☐ Flash
 - ☐ Test
 - ☐ CQN (Q&R)
 - ☐ Packaging
 - ☐ Boards/Cartridge
 - ☐ Automation
 - ☐ Other

2. Concise Title of Invention:

Crack resistant low-k laminate structures

3. Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):

The invention is:

Laminates consisting of brittle low-k layers (e.g., carbon doped oxides) and SiO₂ with compressive stress can significantly improve crack resistance.

Carbon doped oxide (CDO) materials have been considered as an important low-k candidate because of various attractive film properties and they can be deposited in PECVD equipment, similar to traditional oxide films. However, these CDO films can suffer severely from cracking, flaking, and delamination, making them challenging to integrate. A method to improve their crack resistance is to make a laminate structure of CDO and a material with higher toughness, keeping the second material thin so it will not significantly increase the k-value of the whole structure.

The key elements are:

- A. Crack resistance of a brittle low-k material can be significantly improved by laminating the material with a tougher film with compressive stress (such as SiO₂ and SiN).

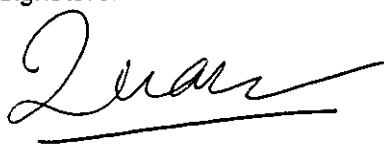
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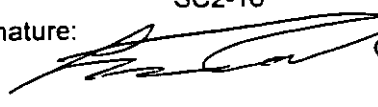
PATENT DATABASE GROUP
INTEL LEGAL TEAMComputer
IP Coordinator
Sherry Wheeler SC1-02
1267

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4. Inventor(s):

Name: Quan Tran SS# 612-52-4736 Empl.# 10581923 M/S: SC1-03
Phone: (408) 765-2341 Fax: (408) 765-2949 Home Address: 2048 Flintbury Ct. San Jose, CA 95148
Citizenship: USA Supervisor Name: Supervisor Phone: 408-765-2116 Supervisor M/S: SC1-03
Group Name: TMG BUM Presenter: Inventor Signature: 
Division Name: ATD
PTD ☐ CTM ☐ CR ☐ X ☐
STTD ☐ CQN ☐
SMTD ☐ TCAD ☐
Other? ☐

Name: Qing Ma SS# 191-64-5381 Empl.# 10071627 M/S: SC1-02
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Citizenship: P.R. China Supervisor Name: Supervisor Phone: 408-765-2369 Supervisor M/S: SC1-03
Group Name: TMG BUM Presenter: Inventor Signature: 
Division Name: ATD
PTD ☐ CTM ☐ CR ☐ X ☐
STTD ☐ CQN ☐
SMTD ☐ TCAD ☐
Other? ☐

Name: Steve Towle SS# 004-68-8725 Empl.# 10523564 M/S: SC2-16
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Citizenship: USA Supervisor Name: Supervisor Phone: 765-2161 Supervisor M/S: SC2-16
Group Name: TMG BUM Presenter: Inventor Signature: 
Division Name: ATD
PTD ☐ CTM ☐ CR ☐
STTD ☐ CQN ☐
SMTD ☐ TCAD ☐
Other? ☐ TME ☐

Name: SS# Empl.# M/S:
Phone: Fax: Home Address:
Citizenship: Supervisor Name: Supervisor Phone: Supervisor M/S:
Group Name: TMG BUM Presenter: Inventor Signature:
Division Name: ATD
PTD ☐ CTM ☐ CR ☐
STTD ☐ CQN ☐
SMTD ☐ TCAD ☐
Other? ☐

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(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)

DATE: 10/4/1999

SUPERVISOR NAME: Harry Fujimoto

Thomas M. Ardeb
THOMAS M. ARDEB FOR HARRY FUJIMOTO

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date:
(Give expected tape out date if applicable): No
7. Has the subject matter of present disclosure been published or will it be published outside of Intel?
If yes, explain and give date: No
8. Has a product using or manufactured using the present disclosure been sold or offered for sale?
If yes, explain and give date: No
9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number: No
10. Explain the problem being addressed by the invention:

This invention addresses the problem of:

Cracking of low-k films.

11. Explain current state of the art (i.e, how the problem is solved today):

Presently the problem described above is solved by:

Brittle low-k films are restricted to thicknesses well below their cracking threshold, often < 1um.

12. Explain technical advantages of the invention over current state of the art:

The technical advantages of this invention are:

1. It will enhance the mechanical integrity of low-k films, preventing films from cracking failure.

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13. a. Is the invention experimentally verified? Yes
b. Is the invention verified with simulation?
c. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):
1. It was experimentally verified. Critical stress needed to crack film improved by 50% (from 80MPa to 120MPa). See attached memo.
 2. The processing technology is standard. Invention could be implemented with a multistep reaction in a PECVD deposition chamber.
 3. It has only a few percent impact on k.

14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

1. Figure 1a shows a brittle low-K film, such as CDO.
2. Figure 1b shows a double layer laminate that has a thin coating on low-k film. The thin coating has larger toughness and is under compressive stress (typical SiO₂ and SiN)
3. Figure 1c shows a 4 layer laminate, which further improves crack resistance.

Referenced sketches/dwg's/diagrams: (use additional page(s))

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15.

Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

Please see attached figures.

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16. Key Supporting Data (1 page limit on separate page):

Please see attached memo.

17. What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):

P860 and beyond.

18. Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: _____ Yes. Chien Chiang _____

19. Any other information IP committee should consider?

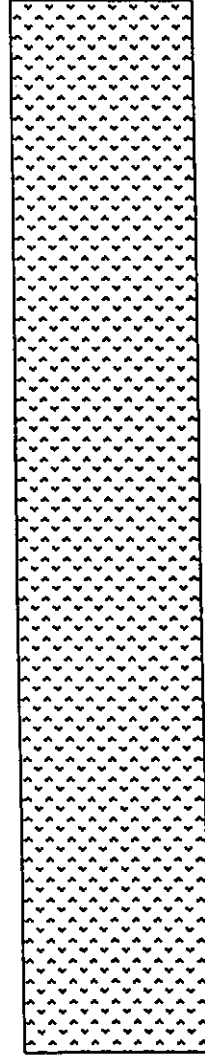
MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

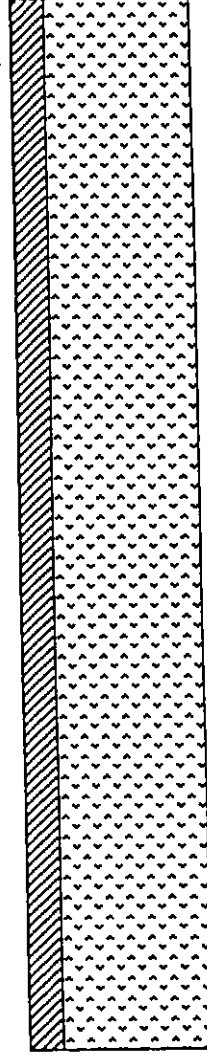
Area	Mentor
Semiconductor Process – device and integration	Mark Bohr, Robert Chau, Krishna Seshan, Greg Atwood
Semiconductor Process – thin films	Ken Cadien, Chien Chiang, John Carruthers
Semiconductor Process – etch/litho	John Carruthers, Peter Silverman, Peter Charvat (etch), Yan Borodovsky (litho)
Circuit Design	Ian Young, Greg Taylor, Clair Webb, Rajesh Galivanche, Greg Atwood
Flash	Greg Atwood, Krishna Seshan
Test	Wayne Needham, Rajesh Galivanche
CQN (Q&R)	Ian Young, Greg Taylor, Clair Webb, John Carruthers, Wayne Needham, Naomi Obinata
Packaging	Ken Kinsman, Jack McMahon
Boards/Cartridge	Leslie Polaski
Automation	Sanjay Natarajan
Other	Ray Werner, Naomi Obinata

Figure 1

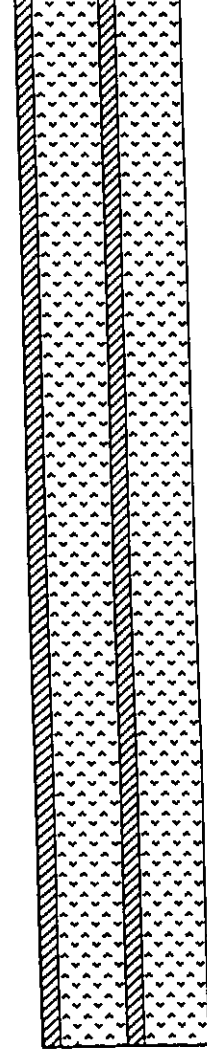
- a. A brittle low-K film, such as CDO.
- b. A double layer laminate that has a thin coating on low-k film. The thin coating has larger toughness and is under compressive stress (typical SiO_2 and SiN)
- c. A 4 layer laminate, which further improves crack resistance.



a



b



c

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first, and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR MAKING A SEMICONDUCTOR
DEVICE HAVING A LOW-K DIELECTRIC LAYER

the specification of which

 x is attached hereto.
 was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign applications for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Priority
Claimed

(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status—patented, pending, abandoned)
----------------------	-------------	--

I hereby appoint Aloysius T. C. AuYeung, Reg. No. 3S,432; William Thomas Babbitt, Reg. No. 39,591; Kent D. Baker, Reg. No. 38,822; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Bravely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No. P39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; [Daniel M De Vos, Reg. No. 37,813; Karen L. Feistharnel, Reg. No. 40,264; David R. Halvorson, Reg. No. 33,395; Brian Don Hickman, Reg. No. 35,894; Eric Ho, Reg. No. P39,711; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Jeffrey D. Jacobs, Reg. No. 40,029; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Dolly M. Lee, Reg. No. 39,742; Michael J.

Marie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H Salter, Reg. No. 35,668, William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 3X,195; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 2S,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; David R. Stevens, Reg. No. 3B,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Alard, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Gary B. Goates, Reg. No. 35,159; Michael Anthony DeSanctis, Reg. No. 39,957; Charles E. Shemwell, Reg. No. 40,171; Edwin A. Sloane, Reg. No. 34,728; and Judith A. Szepesi, Reg. No. 39,393; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 9002E, telephone (310) 207-3800, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468, Mark Seeley, Reg. No. 32,299; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; and Raymond J. Werner, Reg. No. 34,752 of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Mark Seeley, c/o BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Mark Seeley, (408) 765-7382.

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Full Name of Sole/First Inventor Ebrahim Andideh

Inventor's Signature X Date X

Residence 10141 N.W. Priscilla Ct., Portland, OR 97229 Citizenship US
(City, State) (Country)

Post Office Address Same as above

Full Name of Second/Joint Inventor Qing Ma

Inventor's Signature X Qing Ma Date X 2/29/2000

Residence 919 Brentwood Dr., San Jose, CA 95129 Citizenship US
(City, State) (Country)

Post Office Address Same as above

Full Name of Third/Joint Inventor Quan Tran

Inventor's Signature X Quan Tran Date X 03/01/2000

Residence 2048 Flintbury Ct., San Jose, CA 95148 Citizenship US
(City, State) (Country)

Post Office Address Same as above

Full Name of Fourth/Joint Inventor Steve Towle

Inventor's Signature X Steve Towle Date X 3/1/2000

Residence 206 S. Bayview Ave., Sunnyvale, CA 94086 Citizenship US
(City, State) (Country)

Post Office Address Same as above

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first, and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR MAKING A SEMICONDUCTOR
DEVICE HAVING A LOW-K DIELECTRIC LAYER

the specification of which

 x is attached hereto.
 was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

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			<u>Priority Claimed</u>	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
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Full Name of Sole/First Inventor Ebrahim Andideh

Inventor's Signature  Date 2/29/2000

Residence 10141 N.W. Priscilla Ct., Portland, OR 97229 Citizenship US
(City, State) (Country)

Post Office Address Same as above

Full Name of Second/Joint Inventor Qing Ma

Inventor's Signature _____ Date _____

Residence 919 Brentwood Dr., San Jose, CA 95129 Citizenship US
(City, State) (Country)

Post Office Address Same as above

Full Name of Third/Joint Inventor Quan Tran

Inventor's Signature _____ Date _____

Residence 2048 Flintbury Ct., San Jose, CA 95148 Citizenship US
(City, State) (Country)

Post Office Address Same as above

Full Name of Fourth/Joint Inventor Steve Towle

Inventor's Signature _____ Date _____

Residence 206 S. Bayview Ave., Sunnyvale, CA 94086 Citizenship US
(City, State) (Country)

Post Office Address Same as above

Attorney's Docket

ASSIGNMENT

PATENT

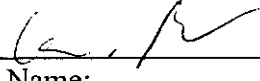
No.: 42390.P8125

(For Execution Prior to Filing Patent Application)

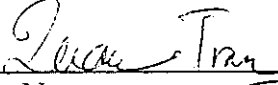
In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, we the undersigned, Ebrahim Andideh, Qing Ma, Quan Tran and Steve Towle, hereby sell, assign, and transfer to Intel Corporation a corporation of Delaware, having a principal place of business at 2200 Mission College Boulevard, Santa Clara, California 95052, ("Assignee"), and its successors, assigns, and legal representatives, the entire right, title, and interest for the United States and all foreign countries, in and to any and all improvements that are disclosed in the application for the United States patent that has been executed by the undersigned prior hereto or concurrently herewith on the dates indicated below and is entitled "METHOD FOR MAKING A SEMICONDUCTOR DEVICE HAVING A LOW-K DIELECTRIC LAYER" and in and to said application and all divisional, continuing substitute, renewal, reissue, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said improvements, and in and to all original and reissued patents that have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application; agree that said Assignee may apply for and receive a patent or patents for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns, and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements' execute all rightful oaths, assignments, powers of attorney, and other papers; communicate to said Assignee, its successors, assigns, and representatives all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible that said Assignee, its successors, assigns, or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements, and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives' and covenant with said Assignee, its successors, assigns, and legal representatives that no assignment, grant, mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Each Inventor: Please Sign and Date Below:

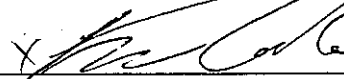
Each Inventor: Please also list the date
that you signed the accompanying
DECLARATION AND POWER OF
ATTORNEY:

X 2/29, 2000 X  Name: _____
Date

X 2/29/2000, 19____
Date

X 03/01, 19 2000 X  Name: _____
Date

X 03/01, 19 2000
Date

X 3/11, 19 2000 X  Name: _____
Date

X 3/11, 19 2000
Date

X _____, 19____ Y _____ Name: _____
Date

X _____, 19____
Date

Attorney's Docket
No.: 42390.P8125

ASSIGNMENT
(For Execution Prior to Filing Patent Application)

PATENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, we the undersigned, Ebrahim Andideh, Qing Ma, Quan Tran and Steve Towle, hereby sell, assign, and transfer to Intel Corporation a corporation of Delaware, having a principal place of business at 2200 Mission College Boulevard, Santa Clara, California 95052, ("Assignee"), and its successors, assigns, and legal representatives, the entire right, title, and interest for the United States and all foreign countries, in and to any and all improvements that are disclosed in the application for the United States patent that has been executed by the undersigned prior hereto or concurrently herewith on the dates indicated below and is entitled "METHOD FOR MAKING A SEMICONDUCTOR DEVICE HAVING A LOW-K DIELECTRIC LAYER" and in and to said application and all divisional, continuing substitute, renewal, reissue, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said improvements, and in and to all original and reissued patents that have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application; agree that said Assignee may apply for and receive a patent or patents for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns, and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements' execute all rightful oaths, assignments, powers of attorney, and other papers; communicate to said Assignee, its successors, assigns, and representatives all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible that said Assignee, its successors, assigns, or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements, and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives' and covenant with said Assignee, its successors, assigns, and legal representatives that no assignment, grant, mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Each Inventor: Please Sign and Date Below:

Each Inventor: Please also list the date
that you signed the accompanying
**DECLARATION AND POWER OF
ATTORNEY:**

<u>FEB. 29</u> , <u>2000</u> Date	<u><i>Ernestine Anselmi</i></u> Name:	<u>FEB. 29, 2000</u> , <u>19</u> Date
_____, 19____ Date	_____ Name:	_____, 19____ Date
_____, 19____ Date	_____ Name:	_____, 19____ Date
_____, 19____ Date	_____ Name:	_____, 19____ Date